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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/026,688	12/27/2001	Kazushi Fujimoto	Q67203	9334

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EXAMINER	
ANYASO, UCHENDU O	
ART UNIT	**PAPER NUMBER**
2675	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/026,688	FUJIMOTO ET AL.	
	Examiner	Art Unit	
	Uchendu O Anyaso	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. **Claims 1-38** are pending in this action.

Claim Rejections - 35 USC ' 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. **Claims 1-5, 9-13, 17-28** and **32-38** are rejected under 35 U.S.C. 102(b) as being anticipated by *Kobayashi et al* (U.S. 5,973,661).

Regarding **independent claim 1**, Kobayashi teaches a method of driving a liquid crystal display device 10 having a plurality of bus lines for transmitting image data (column 7, lines 64-66, figure 1, 2, at 30, 100-1 to 100-6 & OUT1-OUT6), said method comprising: branching original image data having an original data rate into branched plural-systems image data as represented by V comprising plural systems having a converted data rate which is equal to half of said original data rate as represented by signals VP and VN (figure 3A at V, VP, VN; *see also* column 5, lines 21-33).

Furthermore, Kobayashi teaches supplying a source driver circuit 101 with said branched plural-systems image data in synchronizing with at least a clock signal (CLK) having a clock frequency which is a quarter of said original data rate wherein the timing control circuit 52 distributes holder clock signals Sh1 to Sh6 to sampling holders SH1 to SH6 respectively based

on clock signal CLK and horizontal scanning signal SYNC (figure 3A at CLK, Sh1-Sh6, column 5, lines 38-65).

Furthermore, Kobayashi teaches how to allow the source driver to further branch said branched plural-systems image data into gray scale voltage signals by teaching how sampling switches 112-1 to 112-6 pick second image signal train V(1) to V(6) based on timing signals which is represented by sample holder signals Sh1 to Sh6 from shift register 111 such that the sampling switches 112-1 to 112-6 supply image signals V'(1) to V'(6) for driving each pixel units p-1 to p-6 in display area 102 wherein the image signal V'(1) for driving comprises pixel image signal e'(1), e'(7), e'(13) and so on shown in FIG. 3 (*see* column 7, lines 64 through column 8, lines 13; *see also* figure 3A, 3B). Also, when a horizontal scanning signal SYNC is supplied to a gate of thin film transistor 115 via scanning control circuit 103, thin film transistor 115 is switched to ON to accept image signals to be supplied to electrodes of pixels p-1 to p-6 (figure 1 at p-1 to p-6).

Regarding **independent claim 9**, Kobayashi teaches a method of driving a liquid crystal display device 10 (*see* column 4, lines 55-65, figure 1 at 10, 101, 103; *see e.g.*, column 8, lines 7-13, figure 3A).

Furthermore, Kobayashi teaches a timing controller as represented by timing circuit block 20 connected to the image signal processing circuit 30 for generating image data and at least a clock signal (column 5, lines 3-8, figure 1 at 20, 30, CLK).

Furthermore, Kobayashi teaches a plurality of bus lines for transmitting image data and at least a clock signal (column 7, lines 64-66, figure 1, 2, at 30, 100-1 to 100-6 & OUT1-OUT6),

said method comprising: branching original image data having an original data rate into branched plural-systems image data as represented by V comprising plural systems having a converted data rate which is equal to half of said original data rate as represented by signals VP and VN (figure 3A at V, VP, VN; *see also* column 5, lines 21-33).

Furthermore, Kobayashi teaches supplying a source driver circuit 101 with said branched plural-systems image data in synchronizing with at least a clock signal (CLK) having a clock frequency which is a quarter of said original data rate wherein the timing control circuit 52 distributes holder clock signals Sh1 to Sh6 to sampling holders SH1 to SH6 respectively based on clock signal CLK and horizontal scanning signal SYNC (figure 3A at CLK, Sh1-Sh6, column 5, lines 38-65).

Furthermore, Kobayashi teaches how to allow the source driver to further branch said branched plural-systems image data into gray scale voltage signals by teaching how sampling switches 112-1 to 112-6 pick second image signal train V(1) to V(6) based on timing signals which is represented by sample holder signals Sh1 to Sh6 from shift register 111 such that the sampling switches 112-1 to 112-6 supply image signals V'(1) to V'(6) for driving each pixel units p-1 to p-6 in display area 102 wherein the image signal V'(1) for driving comprises pixel image signal e'(1), e'(7), e'(13) and so on shown in FIG. 3 (*see* column 7, lines 64 through column 8, lines 13; *see also* figure 3A, 3B). Also, when a horizontal scanning signal SYNC is supplied to a gate of thin film transistor 115 via scanning control circuit 103, thin film transistor 115 is switched to ON to accept image signals.

Regarding **independent claim 24**, Kobayashi teaches a method of driving a liquid crystal display device 10 (*see* column 4, lines 55-65, figure 1 at 10, 101, 103; *see e.g.*, column 8, lines 7-13, figure 3A).

Furthermore, Kobayashi teaches a timing controller as represented by timing circuit block 20 connected to the image signal processing circuit 30 for generating image data and at least a clock signal (column 5, lines 3-8, figure 1 at 20, 30, CLK).

Also, Kobayashi teaches a serial-to-parallel converting unit by teaching a phase expansion circuit 50 within the image processing circuit for receiving a serially applied train of pixel image signals and generating corresponding plurality of expanded image signal trains in parallel (column 3, lines 17-25, figure 2 at 30, 50).

Furthermore, Kobayashi teaches a plurality of bus lines for transmitting image data and at least a clock signal (column 7, lines 64-66, figure 1, 2, at 30, 100-1 to 100-6 & OUT1-OUT6), said method comprising: branching original image data having an original data rate into branched plural-systems image data as represented by V comprising plural systems having a converted data rate which is equal to half of said original data rate as represented by signals VP and VN (figure 3A at V, VP, VN; *see also* column 5, lines 21-33).

Regarding **claims 2, 5, 10, 13, 25** and **28**, in further discussion of claims 1, 9 and 24, Kobayashi teaches how the number of the systems of the branched plural-systems image data is 2J, where J is a positive integer number (figure 3A at V, VP column 5, lines 21-33).

Regarding **claims 3, 11** and **26**, in further discussion of claims 1, 9 and 24, Kobayashi teaches how the number of said systems of said branched plural-systems image data is 4J, where J is a positive integer number (figure 3A at V, VP, VN, V(1)-V(6); *see also* column 5, lines 21-33).

Regarding **claims 4, 12** and **27**, in further discussion of claims 1, 9 and 24, Kobayashi teaches how the converted data rate is equal to said original data rate as shown by the comparison of e(1) and e'(1), e(2) and e'(2) etc (see figure 3A at VP, VN, V'(1)-V'(6)).

Regarding **claims 17-19, 32-34**, in further discussion of claims 9, 24, Kobayashi teaches a data polarity inversion determination unit by teaching selectors 42a and 42b wherein selector 42a selects positive image signal VP and distributes it to phase expansion circuit 50 while selector 42b selects negative image signal VN such that these selectors 42a and 42b are controlled by control signal from timing control circuit 35 (column 5, lines 24-33, figure 2 at 42a, 42b).

Furthermore, Kobayashi teaches data polarity inversion unit by teaching an inversion circuit 40 for inverting all bits of said branched plural-systems image data in polarity if it is verified that said majority of bits of said branched plural-systems image data is changed in polarity wherein inversion circuit 40 generates two kinds of image signals based on input image signal V, i.e., the normal positive polarity signal of input image signal and the negative polarity signals of inverted input image signal and distribute them to two selectors 42a and 42b (column 5, lines 24-33, figure 2 at 42a, 42b).

Regarding **claims 20, 35**, in further discussion of claims 9 and 24, Kobayashi teaches a first latch circuit as represented by timing circuit block 20 connected to image signal circuit 41 for latching said branched plural-systems image data in synchronizing with said at least a clock signal that is derived from and outputting said branched plural-systems image data as first output data (figure 2 at 20, 41).

Furthermore, Kobayashi teaches a data polarity inversion unit by teaching an inversion circuit 40 for inverting all bits of said branched plural-systems image data in polarity if it is verified that said majority of bits of said branched plural-systems image data is changed in polarity wherein inversion circuit 40 generates two kinds of image signals based on input image signal V, i.e., the normal positive polarity signal of input image signal and the negative polarity signals of inverted input image signal and distribute them to two selectors 42a and 42b (column 5, lines 24-33, figure 2 at 42a, 42b).

Furthermore, Kobayashi teaches a data polarity inversion determination unit by teaching selectors 42a and 42b wherein selector 42a selects positive image signal VP and distributes it to phase expansion circuit 50 while selector 42b selects negative image signal VN such that these selectors 42a and 42b are controlled by control signal from timing control circuit 35 (column 5, lines 24-33, figure 2 at 42a, 42b).

Also, Kobayashi teaches and a second latch circuit as represented by inversion circuit 40 for latching said second polarity inversion signal in synchronizing with said at least a clock signal and supplying said first polarity inversion signal to said first data polarity inversion determination circuit (see column 5, lines 38-49, figure 2, 3A)..

Regarding **claims 21-23** and **36-38**, in further discussion of claims 9 and 24, Kobayashi teaches a third latch circuit as represented by sampling holders (SH1, SH3, SH5) contained in phase expansion circuit 50 for latching said polarity-inverted image data in synchronizing with said at least a clock signal and supplying said polarity-inverted image data to said source driver (see figure 2 at 50, SH1, SH3, SH5).

Furthermore, Kobayashi teaches a fourth latch circuit as represented by sampling holders (SH2, SH4, SH6) contained in phase expansion circuit 50 for latching said first polarity inversion signal in synchronizing with said at least a clock signal and supplying said first polarity inversion signal to said source driver (see figure 2 at 50, SH2, SH4, SH6).

Claim Rejections - 35 USC ' 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claims 6-8, 14-16** and **29-31** are rejected under 35 U.S.C. 103(a) as being unpatentable over *Kobayashi et al* (U.S. 5,973,661) in view of *Yeo* (U.S. 6,097,234).

Regarding **claims 6-8, 14-16** and **29-31**, in further discussion of claims 1, 9 and 24, Kobayashi teaches how a timing circuit block 20 receives source clock signals CLK and distributes control signals to the shift register 111 contained in the source driver (image signal drive circuit 101) (column 5, lines 3-6, figure 1 at 20, 101, 111). However, Kobayashi does not teach how the clock signal comprises two clock signals that are different in phase. On the other

hand, Yeo teaches this concept by teaching a three-phase clock signal generation circuit for a source driver of TFT-LCDs capable of sequentially or simultaneously generating three-phase clock signals for sampling R(red), G(green) and B(blue) data using one clock signal wherein the clock signals are of different phases and the edges of the clock signals serve as triggers to input said image data into said source driver (column 1, lines 5-13; see also column 1, lines 64 through column 2, lines 12, figure 1 at MCLK, 10, 100).

Thus, it would have been obvious to a person of ordinary skill in the art to combine Kobayashi and Yeo because while Kobayashi teaches a method of driving a liquid crystal display device 10 having a plurality of bus lines for transmitting image data (column 7, lines 64-66, figure 1, 2, at 30, 100-1 to 100-6 & OUT1-OUT6), said method comprising: branching original image data having an original data rate into branched plural-systems image data as represented by V (figure 3A at V, VP, VN; *see also* column 5, lines 21-33), Yeo teaches a three-phase clock signal generation circuit for a source driver of TFT-LCDs capable of sequentially or simultaneously generating three-phase clock signals for sampling R(red), G(green) and B(blue) data using one clock signal wherein the clock signals are of different phases and the rising edges of the clock signals serve as triggers to input said image data into said source driver (column 1, lines 5-13; see also column 1, lines 64 through column 2, lines 12, figure 1 at MCLK, 10, 100). The motivation for doing so would have been to provide a three-phase clock signal generation circuit for a source driver of TFT-LCDs capable of sequentially or simultaneously generating three-phase clock signals for sampling R(red), G(green) and B(blue) data using one clock signal (column 1, lines 40-44).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent 5,113,181 to *Inoue et al* for a display apparatus.

U.S. Patent 6,670,942 to *Van Asma et al* for a sampler for a picture display device.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Uchendu O. Anyaso whose telephone number is (703) 306-5934. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steve Saras, can be reached at (703) 305-9720.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Uchendu O. Anyaso

09/04/2004

DENNIS-DOON CHOW
PRIMARY EXAMINER